Exhibit 23

PATENT
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IN THE UNITED STATES PATENT & TRADEMARK OFFICE

Applicant:	Thomas E. Grebs, et al.	)	Examiner: Fetsum Abraham
Serial No.:	10/247,464	)	
Filed:	September 19, 2002	)	Art Unit: 2826
For:	BURIED GATE - FIELD TERMINATION STRUCTURE	)	

AMENDMENT

Commissioner for Patents
P O Box 1450
Alexandria, Virginia 22313-1450

Dear Sir:

In response to the office action mailed May 16, 2003, please amend the above-identified application as follows:

Amendments to the Claims:

In the Claims:

1. (currently amended) A switchable semiconductor power device of the type which controls current conduction based on field effect principles, comprising:

a semiconductor layer having a transistor region including a source/drain formation and a termination region surrounding the transistor region, said termination region including an outer periphery corresponding to an edge of the device; and

a single conductor, configured for connection to a gate voltage supply, including first and second conductor portions with the first conductor portion positioned in the transistor region to control current flow through the source/drain formation and the second conductor portion positioned in the termination region, the second conductor portion ~~including~~:

including a contact for connection to the gate voltage supply; ~~and~~

including a feed comprising conductive material formed in a trench extending along the outer periphery and around the transistor region, said feed electrically connecting the contact with the first conductor portion.; and

acting as a field plate to extend the device breakdown voltage in the termination region.

2. (original) The device of claim 1 further comprising a plurality of additional source/drain formations each configured with the first conductor portion in and about a trench region to provide a voltage-switchable conduction channel for controlling current flow through the semiconductor layer.

3. (original) The device of claim 1 wherein the first conductor portion is formed in a trench.

4. (original) The device of claim 1 further including an isolation trench extending into the semiconductor layer and positioned between the edge of the device and the second conductor portion.

5. (cancelled)

6. (original) The device of claim 1 wherein the transistor region comprises a vertical MOSFET device.

7. (currently amended) A semiconductor structure comprising:

a layer of semiconductor material having an active device region and a peripheral region surrounding the active region;

a transistor device formed in the active region, having a gate region including a gate conductor formed in a first trench, the gate conductor electrically isolated from the semiconductor layer by a relatively thin insulator; and

a second trench formed along the peripheral region and including a second conductor formed therein with a relatively thick insulator positioned to electrically isolate the second trench conductor from the semiconductor layer, said second conductor:

electrically connected to gate conductor of said transistor device;

acting as a field plate to extend the device breakdown voltage in the termination region.

8. (cancelled)

9. (cancelled)

10. (original) The structure of claim 7 wherein the transistor device is a vertical MOSFET.

11. (original) The structure of claim 10 wherein the transistor device comprises a plurality of MOSFET cells each electrically connected to the second conductor in order to simultaneously conduct current through the layer of semiconductor material.

12. (original) The structure of claim 6 wherein the device is an N-channel MOSFET.

13. (original) The method of claim 7 wherein the second trench is as deep or deeper than the first trench.

14. (currently amended) A method for manufacturing a semiconductor device, comprising:

providing on a layer of semiconductor material an active region and a termination periphery region surrounding the active region with a trenched transistor formation in the active region; ~~and~~

forming a trenched gate runner in the termination region along the active region; and

forming first and second conductor regions such that said first and second conductor regions are electrically connected to form a continuous conductor with multiple regions and said first conductor region is in said trenched transistor formation and said second conductor region is said trenched gate runner such that said second conductor also acts as a field plate termination.

15. (original) The method of claim 14 wherein the step of providing the trenched transistor formation includes forming a relatively thin oxide layer therein to provide a gate dielectric and the step of forming the trenched gate runner includes forming a relatively thick oxide layer therein to provide electrical isolation between the trench and the layer of semiconductor material.

16. (original) The method of claim 14 wherein the trenched gate runner extends further into the layer of semiconductor material than the trenched transistor formation.

17. (original) The method of claim 14 wherein the trenched transistor formation includes a gate conductor formed simultaneously with the gate runner by deposition of polysilicon.

18. (currently amended) A method for operating a semiconductor device comprising:

providing a semiconductor layer with an active transistor region and a trenched field plate positioned about the transistor region for increasing breakdown voltage such that said active transistor region and said trenched field plate are electrically connected; and

using the field plate as a conductive feed to control switching of transistors in the active region.

19. (original) A semiconductor structure comprising:

a layer of semiconductor material having an active device region and a peripheral region surrounding the active region;

a transistor device formed in the active region including a plurality of source regions on one surface and drain region on the opposite surface;

a trench having

an outer annular portion disposed in the peripheral region and enclosing the transistor device, the walls and the floor of the outer annular portion lined with

an insulator and the outer annular portion filled with conductive material for forming a field plate around the transistor regions; and

a plurality of elongated inner runners extending in the same direction across the one surface with the source regions and intersecting the outer annular portion at opposite ends of the runners, the runners having their floors and their walls lined with a gate insulating material and the runners filled with a conductor to form a gate structure in the transistor region to control current between the source regions and the drain.

20. (original) The semiconductor of claim 22. wherein the conductor material comprises conductive polysilicon.

21. (original) The semiconductor of claim 21 further comprising a layer of metal on the conductive polysilicon.

22. (original) The semiconductor of claim 20 wherein the insulator in the outer annular portion is thicker than the gate insulator in the runners.

23. (original) The semiconductor of claim 20 wherein a common layer of conductive polysilicon fills the trench.

24. (original) The semiconductor of claim 24 further comprising a second layer of insulator over the polysilicon to cover the walls of the polysilicon in the annular trench and to cover the tops of the runner trenches.

Amendments to the Specification:

In the Brief Description of the Drawings on page 3;

Figures 3A – 3C illustrate a sequence of fabrication steps according to the invention;

Figure 4A is a top view of prior art using planar edge termination and gate runner structures;

Figure 4B is a top view of the invention using buried termination and gate runner structures.

In the first paragraph of the Detailed Description of the Invention on page 4, line 18, delete "while":

The partial cross sectional view of Figure 1 illustrates a P-channel MOSFET device 10 formed in a semiconductor layer 12, including N+ lower layer 14 and N- upper layer 16 which may, for example, be epitaxially grown. The layer 16 has an upper surface 18. A P+ diffusion region 22 extends from the surface 18 into the upper layer 16. An active transistor region 20 of the device 10 (right side of drawing) includes a repetitive pattern of MOS cell structures each having a vertical source/drain formation. For simplicity of illustration only one exemplary MOSFET cell 24 is shown extending through a body region portion of the diffusion region 22. The device 10 will include many MOSFET cells, although the specific design of the cell 24 is exemplary ~~while~~ the invention is not at all limited to any particular type of cell design nor limited solely to MOSFET devices.

In the Detailed Description of the Invention on page 7, line 26:

Figure 4A shows a top view of the prior art using planar edge termination and gate runner structures. Figure 4B shows the top view of the invention using buried termination and gate runner structures. By integrating the termination structure with the gate runner structure there is a reduction in the total die area required to effect both of these functions. For example, the distance from the die edge periphery 52 to the first active trench 28 may be about 20 microns, while for a device of similar rating but with a conventional edge termination structure, the distance from the edge of the die to the first active trench will be on the order of 120 microns. Also, having the termination region 50 include a portion of region 22 there is no need for a

separate implant step, this resulting in a reduction in the number of processing steps required for manufacture of the device. With the termination structure formed in a trench that is simultaneously formed with the gate oxide trench, the overlying surface topography is planar, i.e., not characterized by steps due to oxide formation, and this avoids puddling of photoresist which is known to compromise lithographic image integrity.

Amendments to the Drawing Figures:

Please add new Figure 4A and Figure 4B to the application. The specification has been amended to include brief and detailed descriptions of these new figures

Remarks:

In the Office Action mailed on May 16, 2003, the Examiner rejected claims 19-24 under 35 U.S.C. § 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. The Examiner rejected claims 1-4, 6-8, 10, 11, 14, and 15 under 35 U.S.C § 102(b) as being anticipated by Baliga (5.998,833). The Examiner rejected claims 5, 9, 12, and 18 under 35 U.S.C § 103(a) as being unpatentable over Baliga ('833). Each of the above rejections are addressed below.

In response to the above mentioned Office Action, claims 1, 7, 14, and 18 have been amended and claims 5, 8, and 9 have been cancelled. These changes further clarify the scope and intent of the claims.

The Examiner stated that, in regards to claims 19-24, the structural relationship between the source regions and the gate runner is unclear in the structure of Figure 1. That figure should be read in combination with Figure 2. Note that the first conductor 64 and the second conductor 34 are shown in Figure 1. The sources 38 are adjacent the gates that include the second conductor 34.

Applicant has provided new Figures 4A and 4B which further illustrate the differences between the prior art and the Applicant's invention. Figure 4A illustrates the top view of prior art in which the edge termination is created separately from the gate runner. In contrast, Figure 4B illustrates the top view of the invention in which the edge termination is combined with the gate runner structure. The source regions and the gate runner connect at the termination region. Combining the gate runner with the edge termination allows more space on the die layout for more transistor structures; alternatively the same number of transistors as in the prior art can be fit into a smaller die layout.

In regard to Applicant's claim 1, the invention integrates the field termination with the gate runner in the second conductor region. The claims of the invention provides for gate electrodes, gate feeders and field plate termination, but combines the field plate termination with the gate feeders. The reference fails to show or suggest such a combination of elements.

As for Applicant's claims 3 and 4, the isolation trench is not part of the second conductor. The second conductor is placed ***between*** the isolation trench and the first conductor. The isolation trench is ***between*** the second conductor and the edge of the device. In Baliga '833, the second conductor (136) is an integral part of the isolation trench.

In regard to Applicant's amended claim 7, the invention electrically connects the second conductor in the peripheral region to the gate conductors in the transistor regions. The reference fails to show or suggest that the second conductor is connected to the gate conductors.

Applicant's amended claim 14 is distinguishable from prior art as the first and second conductors are electrically connected to each other. Further the second conductor doubles as a gate runner and a field plate termination. The reference fails to show or suggest that the second conductor serves as both a gate runner and field plate termination.

Applicant's claim 18 integrates the field plate termination with the second conductor gate feeder in the termination region which is electrically connected to the transistor formations. Applicant's disclosure is fundamentally different from prior art on this point as the prior art maintains the field plate termination separate from the second conductor gate feeder.

Respectfully submitted,

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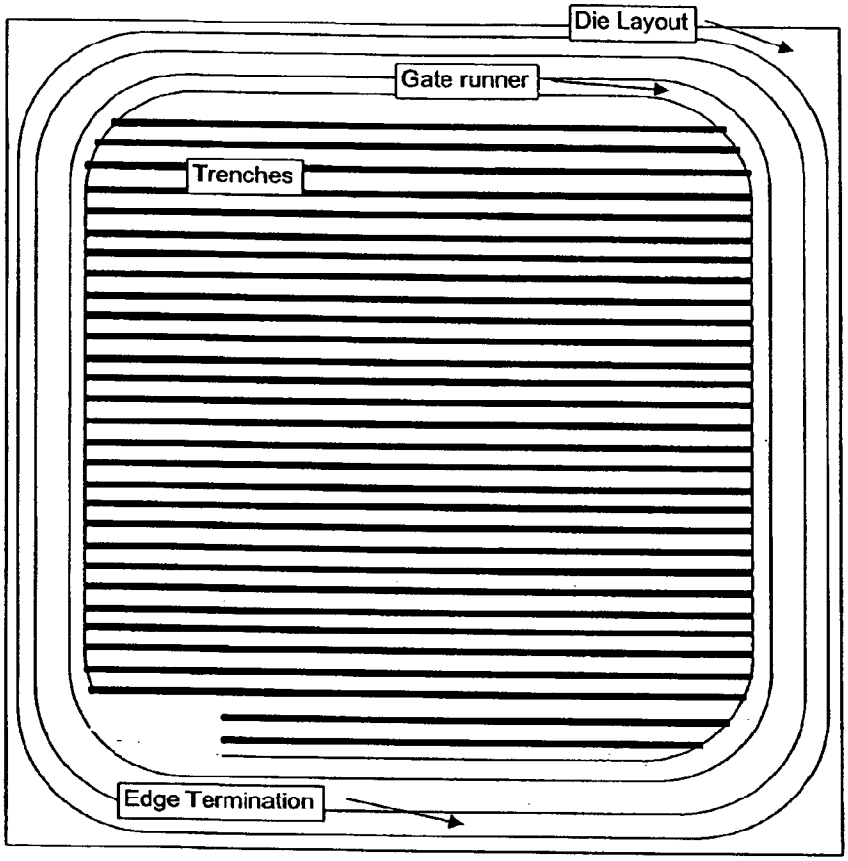

Fig. 4A

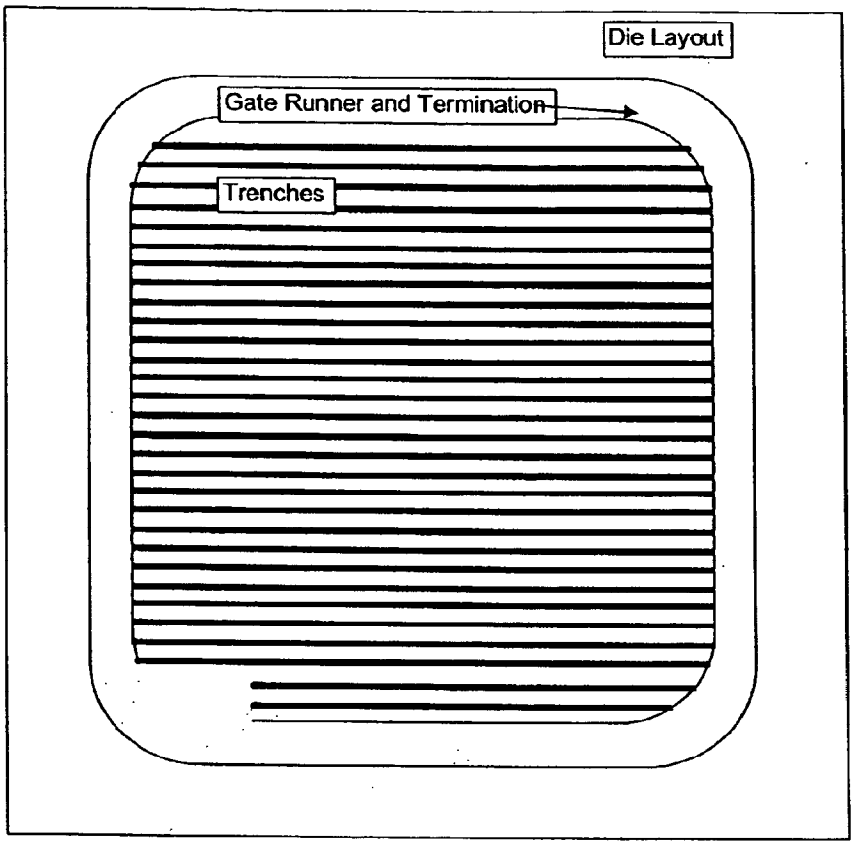

Fig. 4B